changes increase the internal I/O bandwidth by at least a factor of 8. Four internal buses are used to route these internal I/O lines. Increasing the number of I/O lines and then splitting them in the middle greatly reduces the capacitance of each internal I/O line which in turn reduces the column access time, increasing the column access bandwidth even further.

IN THE CLAIMS:

Kindly **cancel** claims 1-150, without prejudice.

Kindly **add** the following claims:

346 C1 --151. A synchronous memory device including an array of memory cells, the synchronous memory device comprises:

clock receiver circuitry to receive an external clock signal;

input receiver circuitry to sample a first operation code synchronously with respect to a transition of the external clock signal;

a programmable register to store a value which is representative of an amount of time to transpire before the memory device outputs data, wherein the memory device stores the value in the programmable register in response to the first operation code; and

output driver circuitry to output data in response to a second operation code, wherein the data is output after the amount of time transpires, and wherein:

the output driver circuitry outputs a first portion of the data synchronously with respect to a rising edge transition of the external clock signal and outputs a second portion of the data synchronously with respect to a falling edge transition of the external clock signal.

152. The memory device of claim 151 wherein the first operation code is included in a control register access packet.

153. The memory device of claim 152 wherein the first operation code and the value are included in the same control register access packet.

154. The memory device of claim 151 wherein the memory device is a synchronous DRAM.

155. The memory device of claim 151 wherein the input receiver circuitry receives the second operation code and address information corresponding to at least one memory cell location of the array of memory cells.

156. The memory device of claim 151 wherein the input receiver circuitry receives at least one of the second operation code and

address information corresponding to at least one memory cell location of the array of memory cells.

157. The memory device of claim 151 wherein the amount of time is representative of a number of clock cycles of the external clock signal.

158. The memory device of claim 151 wherein the input receiver circuitry receives a third operation code, wherein the third operation code initiates a write operation in the memory device.

159. The memory device of claim 158 wherein the input receiver circuitry receives the third operation code and address information corresponding to at least one memory cell location of the array of memory cells.

160. The memory device of claim 151 further including delay lock loop circuitry coupled to the clock receiver circuitry to generate a first internal clock signal, wherein the data is output using the first internal clock signal.

161. The memory device of claim 151 wherein the output driver circuitry outputs the data onto a bus.

162. The memory device of claim 161 wherein the bus includes a set of signal lines used to transmit multiplexed address information, data and control information.

163. A method of operation of a synchronous memory device, wherein the memory device includes an array of memory cells and a programmable register, the method of operation of the memory device comprises:

sampling a first operation code synchronously with respect to an external clock signal;

receiving a binary value wherein the memory device stores the binary value in the programmable register in response to the first operation code wherein the binary value is representative of an amount

of time to transpire before the memory device outputs data in response to a second operation code;

sampling the second operation code; and

outputting data after the amount of time transpires, wherein a first portion of the data is output synchronously with respect to a first transition of the external clock signal and a second portion of the data is output synchronously with respect to a second transition of the external clock signal.

164. The method of claim 163 wherein the second operation code is sampled synchronously with respect to the external clock signal.

165. The method of claim 163 wherein the binary value is representative of a number of clock cycles of the external clock signal.

166. The method of claim 165 further including:

receiving block size information wherein the block size information defines an amount of data to be output in response to the second operation code, wherein the memory device outputs the amount of data after the number of clock cycles of the external clock signal transpire.

~~167. The method of claim 163 further including receiving address information synchronously with respect to the external clock signal.~~

168. The method of claim 163 wherein the address information and the second operation code are included in a read request packet.

169. The method of claim 163 further including receiving precharge information.

170. The method of claim 169 wherein the precharge information includes a binary bit, wherein, after accessing the data from the array ~~of memory cells, the memory device retains contents of a plurality of~~

sense amplifiers for a subsequent memory operation as a result of a first state of the binary bit.

171. The method of claim 163 wherein the first transition of the external clock signal is a rising edge transition and the second transition of the external clock signal is a falling edge transition.

172. The method of claim 171 wherein the first and second transitions of the external clock signal are consecutive transitions of the external clock signal.

173. The method of claim 163 wherein the first operation code is sampled during an initialization sequence after power is applied to the memory device.

174. The method of claim 163 wherein the memory device samples the first operation code from an external bus, and wherein the memory device outputs data onto the external bus.

175. The method of claim 174 wherein the external bus includes a set of signal lines used to transmit multiplexed address information, data and control information.

176. A method of controlling a synchronous memory device by a memory controller, wherein the memory device includes an array of memory cells and a programmable register, the method of controlling the memory device comprises:

issuing a first operation code to the memory device, wherein the first operation code initiates an access of the programmable register in the memory device in order to store a binary value;

providing the binary value to the memory device, wherein the memory device stores the binary value in the programmable register in response to the first operation code;

issuing a second operation code to the memory device, wherein the second operation code instructs the memory device to accept data that is ~~issued by the memory controller~~;

issuing a first portion of the data to the memory device synchronously with respect to a first transition of the external clock signal; and

issuing a second portion of the data to the memory device synchronously with respect to a second transition of the external clock signal.

177. The method of claim 176 wherein the binary value is representative of a delay time to transpire before the memory device samples the data, and wherein the first portion of the data is issued to the memory device after the delay time transpires.

178. The method of claim 176 wherein the binary value is representative of a number of clock cycles of the external clock signal.

179. The method of claim 176 wherein the first transition of the external clock signal is a rising edge transition and the second transition of the external clock signal is a falling edge transition.

180. The method of claim 176 further including:

providing block size information to the memory device, wherein the block size information defines an amount of data to be accepted by the memory device in response to the second operation code.

181. The method of claim 176 further including providing address information to the memory device.

182. The method of claim 181 wherein the address information and the second operation code are included in a write request packet.

183. The method of claim 176 wherein the first operation code and the data are issued onto an external bus.

184. The method of claim 183 wherein the external bus includes a set of signal lines used to transmit multiplexed address information, data and control information.

185. The method of claim 176 wherein the second operation code includes precharge information.

186. A synchronous memory device, wherein the memory device includes an array of memory cells, the memory device comprises:

input receiver circuitry to sample a first operation code synchronously with respect to an external clock signal;

a programmable register to store a binary value in response to the first operation code, wherein the binary value is representative of an amount of time to transpire before the memory device outputs data; and

output driver circuitry to output data in response to a second operation code and after the amount of time transpires, wherein a first portion of the data is output synchronously with respect to a first transition of the external clock signal and a second portion of the data is output synchronously with respect to a second transition of the external clock signal.

187. The memory device of claim 186 wherein the binary value is representative of a number of clock cycles of the external clock signal.

188. The memory device of claim 187 wherein the binary value is representative of a fractional number of clock cycles of the external clock signal.

188. The memory device of claim 186 wherein the first transition of the external clock signal is a rising edge transition and the second transition of the external clock signal is a falling edge transition.

189. The memory device of claim 188 wherein the first and second ~~transitions of the external clock signal are consecutive transitions.~~

190. The memory device of claim 189 wherein the first operation code and the binary value are included in a packet.

191. The memory device of claim 190 wherein the first operation code and the binary value are included in the same packet.

192. The memory device of claim 186 further including delay lock loop circuitry to generate a first internal clock signal, wherein the data is output using the first internal clock signal.

193. The memory device of claim 186 wherein the input receiver circuitry receives address information corresponding to at least one memory cell location of the array of memory cells.

194. The memory device of claim 186 wherein the output driver circuitry outputs data onto an external bus having a set of signal lines used to transmit multiplexed address information, data and control information.

195. The memory device of claim 194 wherein the input receiver circuitry samples the first operation code from the external bus.

196. The memory device of claim 186 wherein the output driver circuitry and the input receiver circuitry are connected to a common pad.

197. The memory device of claim 186 wherein the memory device is a synchronous DRAM.--